ABSTRACT OF THE DISCLOSURE

A CMOS process for double vertical channel thin film transistor (DVC TFT). This process fabricates a CMOS with a double vertical channel (DVC) structure and defines the channel without an additional mask. The DVC structure of the CMOS side steps the photolithography limitation because the deep-submicrometer channel length is determined by the thickness of gate, thereby decreasing the channel length of the CMOS substantially.